What is Claimed is

1. A memory module, comprising:

a mounting substrate;

a plurality of integrated memory components, the components arranged on the mounting substrate;

a refresh control circuit, the refresh control circuit being arranged separately from the memory components on the mounting substrate, an output of the refresh control circuit being connected to the plurality of integrated memory components;

the mounting substrate having connections for supplying address and command signals,

an input of the refresh control circuit being connected to the connections for supplying the address and command signals,

the refresh control circuit being designed such that, when address or command signals which have been generated outside the memory module are supplied, the refresh control circuit receiving and processing the signals, based on the access information obtained therefrom, the refresh control circuit independently generating a refresh command for refreshing the contents of memory cells in a selected one of the memory components, and the refresh control circuit transmitting the command to the selected memory component.

2. The memory module as claimed in claim 1, wherein the refresh control circuit evaluates the command signals with regard to a defined command pattern and

independently determines therefrom the point in time at which a refresh command will be sent.

3. The memory module as claimed in claim 2, wherein the refresh control circuit evaluates the command signals by a heuristic algorithm.

4. The memory module as claimed in claim 1, wherein an adjustable time value has been set in the refresh control circuit, the time value determining the time within which the contents of memory cells in a corresponding memory component are to be refreshed, and the refresh control circuit sending a refresh command based on the adjustable time value.

5. The memory module as claimed in claim 1, wherein

the memory components each having a memory cell array organized in the form of a matrix, the array having rows and columns, and

the refresh control circuit ascertaining which rows in a selected memory component have not been accessed in a predefined period of time and, based on this evaluation, independently the refresh control circuit determining the point in time at which a refresh command will be sent.

6. The memory module as claimed in claim 5, wherein

the memory module has a respective set of counter circuits for independently operated units of rows, the individual counter circuits in a set being associated with a respective different row in the corresponding unit of rows,

the respective counter circuit being reset when the associated row is accessed,

the refresh control circuit evaluating the counter circuits with respect to the count and, the refresh control circuit based on this evaluation, independently determining the point in time at which a refresh command will be sent.

7. The memory module as claimed in claim 1, wherein the refresh control circuit is arranged within a semiconductor chip, the semiconductor chip being separate from the memory components.

8. The memory module as claimed in claim 1, wherein the input connection of the refresh control circuit is connected to a contact strip on the memory module.

9. The memory module as claimed in claim 1, wherein the memory module is in the form of a DIMM module arrangement.

10. The memory module as claimed in claim 1, wherein the memory components in the memory module are dynamic read/write memories.

11. A memory module, comprising:

a mounting substrate;

a plurality of integrated memory components, the components being arranged on the mounting substrate;

a refresh control circuit, the refresh control circuit being arranged separately from the memory components on the mounting substrate, an output of the refresh control circuit being connected to the plurality of integrated memory components;

the mounting substrate having connections for supplying address and command signals,

an input of the refresh control circuit being connected to the connections for supplying the address and command signals,

the refresh control circuit being designed such that, when address or command signals which have been generated outside the memory module are supplied, the refresh control circuit receiving and processing the signals, based on the access information obtained therefrom, the refresh control circuit independently generating a refresh command sequence for refreshing the contents of memory cells in a selected one of the memory components, and the refresh control circuit transmitting the command sequence to the selected memory component.

12. The memory module as claimed in claim 11, wherein the refresh control circuit evaluates the command signals with regard to a defined command pattern and independently determines therefrom the point in time at which a refresh command sequence will be sent.

13. The memory module as claimed in claim 12, wherein the refresh control circuit evaluates the command signals by a heuristic algorithm.

14. The memory module as claimed in claim 11, wherein an adjustable time value has been set in the refresh control circuit, the time value determining the time within which the contents of memory cells in a corresponding memory component are to be refreshed, and the refresh control circuit sending a refresh command sequence based on the adjustable time value.

15. The memory module as claimed in claim 11, wherein

the memory components each having a memory cell array organized in the form of a matrix, the array having rows and columns, and

the refresh control circuit ascertaining which rows in a selected memory component have not been accessed in a predefined period of time and, based on this evaluation, independently the refresh control circuit determining the point in time at which a refresh command sequence will be sent.

16. The memory module as claimed in claim 15, wherein

the memory module has a respective set of counter circuits for independently operated units of rows, the individual counter circuits in a set being associated with a respective different row in the corresponding unit of rows,

the respective counter circuit being reset when the associated row is accessed,

the refresh control circuit evaluating the counter circuits with respect to the count and, the refresh control circuit based on this evaluation, independently determining the point in time at which a refresh command sequence will be sent.

17. The memory module as claimed in claim 11, wherein the refresh control circuit is arranged within a semiconductor chip, the semiconductor chip being separate from the memory components.

18. The memory module as claimed in claim 11, wherein the input connection of the refresh control circuit is connected to a contact strip on the memory module.

19. The memory module as claimed in claim 11, wherein the memory module is in the form of a DIMM module arrangement.

20. The memory module as claimed in claim 11wherein the memory components in the memory module are dynamic read/write memories.